Roll No. ..... Total Pages : 2

BT-7/D-21 **47008**

VLSI DESIGN

Paper : ECE-401E

Opt. (i)

Time : Three Hours] [Maximum Marks : 100

Note : Attempt *five* questions in all, selecting at least *one* question from each unit.

UNIT–I

1. (a) List and explain various design rules. 10

(b) Derive an expression for Drain to Source current in the saturated region for nMOS. 10

2. (a) Explain with diagrams the fabrication process sequence of CMOS fabrication. 10

(b) Draw layout and stick diagram for 3-input nMOS NAND gate. 10

UNIT–II

3. (a) Design and explain 4 : 1 multiplexer. 10

(b) List and explain various layout methodologies. 10

4. (a) Design logic function block of Four-line Gray code to Binary code converter. 10

(b) Describe the concept of packaging with illustrations. 10

UNIT–III

5. (a) Discuss ratio cut approach used to solve partitioning problem. 10

(b) Explain various types of sequential approaches to global routing. 10

6. (a) Define placement. List and explain various types of placement techniques. 10

(b) Describe Lee-Moore algorithm to find a shortest route if the net has two terminals. 10

UNIT–IV

7. Explain various delay models in detail. 20

8. Describe any two of the following :

(a) Timing driven Placement. 10

(b) Via minimization. 10

(c) Power Minimization. 10