10/05/2019

Roll No. .....
Printed Pages : 2

37008

BT-7 / M-19

VLSI DESIGN

Paper–ECE-401-E

Option-I

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt **five** questions in all, selecting at least **one** question from each unit.*

Unit–I

1. (a) Explain with diagrams the fabrication process sequence of nMOS fabrication. 10

   (b) Derive the expression for Drain to Source current in the non-saturated region for nMOS. 10

2. (a) Explain with diagrams the fabrication process sequence of CMOS fabrication. 10

   (b) Draw layout and stick diagram for 3-input nMOS NOR gate. 10

Unit–II

3. (a) Explain the rise-time and fall-time estimation of CMOS inverter delays. 10

   (b) List and describe various algorithmic paradigms involved in the various VLSI problems. 10

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4. (a) Design logic function block of Four-line Gray code to Binary code converter. 10

(b) Describe the computational complexity of VLSI problems. 10

Unit–III

5. (a) Define partitioning. Also, explain Fiduccia-Mattheyses Heuristic method of partitioning. 10

(b) Describe Lee-Moore algorithm to find a shortest route if the net has two terminals. 10

6. (a) Define floorplanning. List and explain various types of floorplans. 10

(b) Explain slicing placement and non-slicing placement topologies used in Detailed Routing. 10

Unit–IV

7. Explain with example zero slack algorithm in detail. 20

8. Describe the following : 20

(a) Weight-based Placement

(b) Clock Skew Problem

(c) Unconstrained *Via* Minimization

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