Roll No. .....

34005

Printed Pages : 2

BT–4 / M–19

DIGITAL ELECTRONICS

Paper–ECE–204 E

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt any **five** questions, selecting at least **one** question from each unit.*

Unit–I

1. Write the minimizing procedure followed in Q-M method. Using Q-M method, obtain the minimal expression for $F = \sum m(1, 2, 3, 6, 7, 8, 9, 13, 15) + d(10, 11, 12, 14)$. Also realise the expression using NAND gate only. 20

2. (a) Describe and design Excess 3 code converter. 10

(b) Implement the Boolean expression of X-OR gate using NAND and NOR gates. 10

Unit–II

3. (a) Differentiate between a flip flop and a Latch. Explain the working of J-K flip flop. Also explain the problem associated with JK flip flop. 10

(b) Draw a diagram for 5 bit ring counter using J K flip flop. Explain its working with the help of timing diagram. 10

4. (a) Design a full adder. What is difference between a binary adder and a BCD adder ? 10

(b) What is demultiplexer ? Explain the working of 1:n demultiplexer using logic diagram. 10

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Unit–III

5. (a) Write in detail the characteristics of digital logic gates. Explain them. 10

   (b) Explain working of CMOS NAND gate. 10

6. (a) Explain the working of ECL inverter. What are drawback of ECL logic gates ? 10

   (b) What is the meaning of Tristate logic ? Draw diagram of TTL NAND gate and explain its working. 10

Unit–IV

7. Write a short note on :

   (a) FPGA

   (b) ROM. 20

8. (a) List the specifications of D/A converters. Explain weighted resistor D/A converter. 10

   (b) Explain the working of dual slope A/D converter. 10

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