Roll No. .....

Total Pages : 04

BT-5/D-18 35110

VLSI TECHNOLOGY

ECE-305N

Time : Three Hours] [Maximum Marks : 75

Note : There are eight questions in all organized in four sections and each section is having two questions from each of the four Units. Attempt *Five* questions in all, selecting at least *one* question from each Unit.

Unit I

1. (a) Explain briefly the steps involved in wafer preparation after the growth of crystal. 8

   (b) Explain briefly the fabrication steps of *p-n* diode. 7

2. (a) What is the significance of clean room ? Is there any classication for the clean room ? Explain. 4

   (b) What do you understand by surface contamination ? How are these harmful ? What should we do to remove these ? 6

(c) Why the isolation is required between adjacent devices ? Explain, how it can be accomplished ? 5

Unit II

3. (a) Explain the growth techniques and kinetics of this oxide growth. What are the important properties exhibited by thin oxides ? 6

(b) Why pre-oxidation cleaning is required ? How can it be done ? 4

(c) What do you undersand by oxide stress ? Why is it important to deal with this oxide stress ? Explain the remedies required for this. 5

4. (a) What are the factors responsible for the redistribution of dopants at the interface after oxide growth ? Explain. 6

(b) What are important properties of wet oxidation and dry oxidation ? 4

(c) How many basic isolation techniques used in VLSI circuits ? Explain with suitable diagram. 5

Unit III

5. (a) Diffusion is basically an atomic movement of diffusants in crystal lattice. Which atomic diffusion models are followed by the diffusion process ? Illustrate with diagrams and expressions the compete diffusion process. **10**

   (b) Explain, how ion implantation is different from diffusion techniques used for the insertion of dopants into the substrate. **5**

6. (a) What is the importance of ion-stopping mechanism ? How many ion-stopping mechanisms are there ? Explain. **8**

   (b) What is the significance of annealing ? What do you understand by annealing temperature ? Explain, how the annealing temperature affect the dose of dopants ? **7**

Unit IV

7. (a) Why lithographic exposure tool is used ? Explain which parameters decide the performance of exposure tool ? Describe the optical exposure methods in detail. **8**

(b) Explain with suitable diagrams the NMOS fabrication process steps. 7

8. (a) How many types of CVD techniques are used for metallization ? Explain APCVD. 5

(b) What do you understand by Lift-off technique ? State the difference between optical lithography and lift-off technique with the help of pattern transfer diagrams. 7

(c) Draw the basic fabrication process steps for the Schottky diode. 3

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