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BT-4/M-21 **44005**

DIGITAL ELECTRONICS (NEW)

Paper–ECE-204E

Time : Three Hours] [Maximum Marks : 100

Note : Attempt *five* questions in all, selecting *one* question from each Unit.

UNIT–I

1. (a) Convert the following into binary, BCD and excess three codes : 24, 356, 71. 5

(b) Implement the Boolean expression of X-OR and AND gate using NOR gates. 5

(c) Perform the following operation : (a) 45-28 using 2's compliment (b) 15-36 using 1's compliment. 5

(d) Prove the following using Boolean algebric theorems :

$$\bar{A}\,BC + A\,\bar{B}\,C + AB\,\bar{C} + ABC = AB + BC + CA$$

$$(A + B)\,(C + D) = \overline{\overline{(A + B)} + \overline{(C + D)}}.$$ 5

2. (a) Minimize the following expression using K-Map and realist the obtained expression using NAND gates only :

$F(A,B,C,D) = \Sigma m(1,3,5,6,7,13,14,15) + d(0,2,8,9)$ 10

(b) Use Q-M method to minimize $f(A,B,C,D,E) = \Sigma m(0,1,2,5,7,11,15,16,19,21,23,26,28,31)$. 10

UNIT–II

3. (a) What is a multiplexer? Explain the logic diagram and working of 4 : 1 Multiplexer in detail. 6

(b) Explain designing and working of 4 bit BCD adder. 8

(c) Design 8 : 3 encoder. 6

4. (a) Design a three bit synchronous counter. 8

(b) What are flip-flops? Explain race around condition of JK flip-flop. Also describe how it is removed by master slave flip-flop? 8

(c) Explain working of register as ring counter. 4

UNIT–III

5. (a) Write brief note on characteristics of digital logic gates. 10

(b) Explain the working of CMOS NAND and CMOS OR gate. 10

6. (a) Describe working of TTL NAND gate. Explain tri state condition of TTL. 12

(b) Explain how TTL logic gates can be interfaced with CMOS logic gates. 8

UNIT–IV

7. (a) Write down the specification of A/D converters. Explain. 8

(b) Explain the working of R-2R D/A converter. Mention its limitations. 12

8. Explain the working of (i) counting ADC (ii) Dual slope ADC. 20
