

Roll No.

Total Pages : 3

MCA/D-17

10310

COMPUTER ORGANIZATION

Paper : MCA-14-12

Time : Three Hours]

[Maximum Marks : 80

Note : Attempt *five* questions in all. Q. No. 1 is compulsory. Attempt *four* more questions selecting *one* question from each unit.

Compulsory Question

1. Answer the following questions in brief :

- (a) Explain the difference between positive edge triggered and positive level triggered D Latch with the help of truth, tables.
- (b) Distinguish between memory mapped and isolated I/O.
- (c) Explain the terms with respect to floating point numbers: overflow, precision, NaN, normalization and biasing.
- (d) What are pros and cons of write-through and write-back cache designs ? (4×4=16)

UNIT-I

2. (a) What is shift register? Design a 4-bit left shift register and explain its working with the help of its truth table.
- (b) What is 4-variable K-map? Construct the K-map for the Boolean equation: $w'x'y'z + w'xy' + wy'z' + wxy'z + wyz'$. (8+8=16)

3. (a) Design a 1-bit comparator circuit with propagated input and then use it to design 4-bit comparator circuit.
- (b) What is sequential circuit? Explain the working of JK flip-flop. (8+8=16)

UNIT-II

4. (a) What is ROM? Explain internal two-dimensional organization of 8×2 ROM chip.
- (b) What is CPU? Explain the CPU organization with the help of its block diagram. (8+8=16)
5. (a) Design a simple computer system with 16 bit address bus and 8 bit data bus which uses isolated I/O. It has $8K \times 8$ RAM, $8K \times 8$ ROM and bidirectional I/O device. Show the design with all required signals and logic.
- (b) For $X = 1101\ 1001\ 0011\ 1100$, show the results of the following operations: shr(X), cil(X), ashl(X), dshl(X). (8+8=16)

UNIT-III

6. (a) Design data path for CPU registers AR, PC, DR, AC, IR for simple CPU with 6 bit address, 4 instructions and 64 byte memory.
- (b) Design a microcoded control unit for simple CPU using horizontal microcode. Make your own assumptions needed for the design. (8+8=16)

7. (a) Write the RTL code for floating point multiplication and division algorithm.
- (b) Write short note on IEEE 754 floating point standard.
- (8+8=16)

UNIT-IV

8. (a) Explain the direct mapping scheme used in cache memory. What are its limitations?
- (b) What is virtual memory? Explain conversion of logical address into physical address using page table.
- (8+8=16)
9. (a) Explain destination-initiated data transfer using handshaking with the help of suitable diagram.
- (b) What is Daisy chaining method of prioritizing of interrupts? Explain its hardware implementation.
- (8+8=16)