Roll No. .....

Total Pages : 02

BT-7/D-18 37008

VLSI DESIGN

ECE-401-E

Time : Three Hours] [Maximum Marks : 100

Note : Attempt *Five* questions in all. selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. (a) Explain, with diagrams, the sequence involved in fabrication of CMOS circuits. **12**

   (b) Draw the layout and stick diagrams for Y = (A.B).C using CMOS. **8**

2. (a) What are lambda based design rules ? Discuss in brief. **10**

   (b) What are the DC characteristics of the CMOS Inverter ? Discuss in brief. **10**

Unit II

3. (a) What are the different layout environments ? Discuss in brief. **10**

(b) Design a 2 input NAND gate using CMOS and draw its stick diagrams. **10**

4. (a) What are PLAs ? Discuss in brief. **10**

(b) What are the various layout rules ? Discuss. **10**

Unit III

5. (a) What is partitioning ? Discuss heuristic method for partitioning. **10**

(b) Discuss rectangular dual graph approach to floor planning. **10**

6. (a) What is placement in ICs ? Discuss resistive placement based method. **10**

(b) Discuss Steiner Trees based routing method. **10**

Unit IV

7. (a) What are the various types of delays in ICs ? Discuss different delay models. **12**

(b) Discuss in brief the routing methods in FPGAs. **8**

8. (a) Discuss Global routing models in ICs. **12**

(b) Discuss in brief power minimization methods for ICs. **8**