Roll No.

Total Pages : 04

BT-3/D-20 43158 DIGITAL ELECTRONICS AND LOGIC DESIGN ES-217A

Time : Three Hours]

[Maximum Marks : 75

Note : All questions in Part A and Part B are compulsory. Attempt any *four* questions from Part C selecting *one* question from each Unit.

Part A

15

- 1. Answer the following questions : $5 \times 3=15$
 - (i) State and explain De Morgan's theorem. Explain designing of OR gate using NAND gates.
 - (ii) Express 456 and 272 in BCD code, Excess 3 and Gray code.
 - (iii) Explain designing of 4 bit gray to binary code converter.
 - (iv) State the difference between positive edge triggering, negative edge triggering and level triggering of flipflops.
 - (v) Draw and explain working of sampling and hold circuit.

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Part B

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- 2. Perform the following operations :
 - (i) $(27)_2 + (53)_2$
 - (ii) $(34 48)_2$ using BCD arithmetic
 - (iii) Simplify (A + B)(A' + C) to minimum number of literals. Implement the obtained expression using And, OR, Inverter logic.

3. Explain the designing of full adder. 5

- Draw a diagram for 5 bit ring counter using JK flip-flop.
 Explain its working with the help of timing diagram. 5
- Draw the diagram of R-2 R ladder D/A Converter. Explain its working.
 5

Part C 40

Unit I

6. Using Q-M method, obtain the minimal expression for $F = \Sigma m \{2, 4, 6, 7, 8, 13, 15\} + d(10, 11, 12, 14)$. Also realize the expression using NAND gate only. 10

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- 7. Reduce the following expressions using K-Map :
 - (a) $F = \Pi M(1, 2, 5, 6, 8, 9, 10)$
 - (b) $f = \Sigma(0, 1, 4, 7, 13, 14) + d(5, 8, 15).$

Realise the obtained expressions using NAND/NOR logic.

10

Unit II

8.	(a)	State and explain the working of BCD adder with	1
		its logic diagram.	6
	(b)	Design a octal to binary encoder.	1
9. What do you mean by multiplexer ? Explain the		t do you mean by multiplexer ? Explain the working	3
	of n	: 1 mux. Implement the function $F(A, B, C, D) =$	=
	Σ(0,	1, 3, 4, 8, 9, 13) using 8×1 mux.	D

Unit III

- 10. (a) Explain the working of JK flip-flop. What is race around condition in JK flip-flop ? How can it be solved by master slave flip-flop ?
 - (b) Design an asynchronous mod-10 counter. Use JK flip-flop for designing the counter. 10

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11. What do you mean by register ? Draw the logic diagram of universal shift register. Explain its working. 10

Unit IV

- 12. Draw and explain the working of dual slope type A/D converter.10
- 13. What is difference between PLA and PAL ? Implement the following Boolean functions using PLA :

F1(A, B, C) =
$$\Sigma m(1, 2, 4, 6)$$
. $f 2(A, B, C) = \Sigma m(0, 1, 5, 7)$,
 $f 3(A, B, C) = \Sigma m(1, 2, 3, 5, 7)$. 10

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